RESPONSE-BASED ANALOG-TO-DIGITAL CONVERSION APPARATUS AND METHOD

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a continuation of and claims priority to United States *, is now a U.S. Patent 6,816,096,* Patent Application Number 10/421,129 entitled "Response-Based Analog-To-Digital Conversion Apparatus and Method and filed on April 23, 2003 for Donald T. Comer and Darren S. Korth, which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0002] This invention relates to devices, methods, and systems for conducting analog-to-digital conversions. Specifically, the invention relates to devices, methods, and systems for conducting analog-to-digital conversions using analog comparators.

DESCRIPTION OF THE RELATED ART

[0003] A flash or parallel analog-to-digital (A/D) converter is useful for high-speed applications due to its single clock cycle conversion capability. Typical applications include data acquisition, video capture, video compression, and the like.

[0004] The architecture for a classical flash A/D converter is described in a variety of tutorial sources, including D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley and sons, New York, 1997, chapter 13. As depicted in Figure 1, a classic A/D architecture 100 for a parallel A/D converter employs a resistor string 110, a comparator bank 120, a digital encoder 125, and an output register 150. In the depicted architecture, the digital encoder 125 comprises a one-high encoder 130 and a binary encoder 140.

As depicted, conversion of an analog input signal (not shown) begins on the rising edge of a conversion clock 102. A delayed version of the conversion clock 102 is provided by the delay element 170 as the delayed conversion clock 172. In the depicted embodiment, the delayed conversion clock 172 is used to latch the digital code 142 into the output register 150

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